Claim Amendments

1-5 (canceled).

6. (currently amended) A memory system comprising:

a memory comprising first and second groups of dynamic memory cells, each cell storing a bit;

an access circuit connected to the memory to access, during an access cycle, a selected one of:

a first set of the bits stored in said first group of said memory cells; and

a second set of the bits stored in said second group of said memory cells;

an error detection circuit connected to the access circuit and said memory to detect an error in a bit accessed during said access cycle, comprising:

a first error detection circuit to detect an error in a bit of said first set of accessed bits; and

a second error detection circuit to detect an error in a bit of said second set of accessed bits; and

a scrub circuit connected to the memory to scrub, during a scrub cycle, a selected one of:

said first set of the bits stored in said first group of said memory cells; and

said second set of the bits stored in said second group of said memory cells.

7. (original) The memory system of claim 6 wherein said first and second error detection circuits also correct said bit errors, respectively.

8. (original) The memory system of claim 6 wherein said first and second subsets of said accessed bits are comprised of equal numbers of said bits.

9. (original) The memory system of claim 6 wherein said first and second subsets of said accessed bits are comprised of different numbers of said bits.

10. (canceled).

11. (currently amended) The memory system of claim ~~10~~ 6 wherein said access cycle and said scrub cycle are non-overlapping.

12. (currently amended) The memory system of claim ~~10~~ 6 wherein said access cycle overlaps said scrub cycle, and wherein, during said access cycle, said access circuit accesses said selected one of said first and second sets of bits, and, during said scrub cycle, said scrub circuit scrubs the other of said selected first and second sets of bits.

13. (currently amended) The memory system of claim ~~10~~ 6 wherein the memory system comprises an integrated circuit.

14. (previously presented) A memory system comprising:

a memory comprising a plurality of dynamic memory cells arranged in a plurality of planes of rows and columns, each cell storing a bit and corresponding memory cells of each plane forming respective stacks;

an access circuit connected to the memory to access, during said access sequence, all of the bits stored in all of said planes of said memory cells; and

an orthogonal error detection circuit connected to the access circuit and said memory to detect an error in a bit accessed during said access sequence, comprising:

a row error detection circuit to detect an error in a bit of a row of said accessed bits;

a column error detection circuit to detect an error in a bit of a column of said accessed bits; and

a stack error detection circuit to detect an error in a bit of a stack of said accessed bits.

15. (previously presented) The memory system of claim 14 wherein said first, second and third error detection circuits also correct said bit errors, respectively.

16. (cancelled).

17. (previously presented) The memory system of claim 14 wherein the stack error detection circuit comprises a parity check circuit.

18. (previously presented) The memory system of claim 14 wherein the stack error detection circuit comprises a RAEDAC unit.

19. (original) The memory system of claim 14 wherein the column error detection circuit comprises a parity check circuit.

20. (original) The memory system of claim 14 wherein the column error detection circuit comprises a RAEDAC unit.

21. (original) The memory system of claim 14 wherein the row error detection circuit comprises a parity check circuit.

22. (original) The memory system of claim 14 wherein the row error detection circuit comprises an EDAC unit.

23. (original) The memory system of claim 14 wherein the memory system comprises an integrated circuit.

24. (currently amended) A circuit for use in a memory system comprising:

a memory comprising a plurality of dynamic memory cells arranged in a plane of m rows and n columns, each cell storing a bit;

an access circuit connected to the memory to access, during an access cycle, all of the bits stored in a selected one of said rows; and

a row error detection circuit connected to the access circuit and said memory to detect an error in a bit of said row of said accessed bits;

the circuit comprising:

a parity generation circuit connected to said memory to generate, during each access cycle in which any of said accessed bits are stored, n parity bits, each related to all m bits stored in respective one of said columns, wherein each parity bit is changed only if a respective bit to be stored is different from the corresponding stored bit.

25. (original) The circuit of claim 24 further comprising:

a parity check circuit connected to said memory and to said parity generation circuit to detect an error in a bit of a column of said accessed bits using said parity bits.

26. (original) The circuit of claim 25 further comprising:

an error correction circuit coupled to the memory and to the parity check circuit to correct said detected column bit error.

27. (currently amended) ~~The~~ A circuit ~~of claim 24 wherein the parity generation circuit generates~~ for use in a memory system comprising:

a memory comprising a plurality of dynamic memory cells arranged in a plane of m rows and n columns, each cell storing a bit;

an access circuit connected to the memory to access, during an access cycle, all of the bits stored in a selected one of said rows; and

a row error detection circuit connected to the access circuit and said memory to detect an error in a bit of said row of said accessed bits;

the circuit comprising:

a code generation circuit connected to said memory to generate, during each access cycle in which any of said accessed bits are stored, a plurality of check bits, each related to a unique combination of at least two of said bits stored in a respective one of said columns, wherein each check bit is changed only if a respective bit to be stored is different from the corresponding stored bit.

28. (original) The circuit of claim 27 further comprising:

an error detection circuit connected to said memory and to said ~~parity~~ code generation circuit to detect an error in a bit of a column of said accessed bits using said ~~parity~~ check bits.

29. (currently amended) The circuit of claim 28 further comprising:

an error correction circuit coupled to the memory and to the ~~parity check~~ error detection circuit to correct said detected column bit error.

30. (original) The circuit of claim 29 further characterized as an integrated circuit, random access error detection and correction (RAEDAC) unit.

31. (previously presented) A random access error detection and correction (RAEDAC) unit for detecting and correcting errors in an ordered bit string of predetermined length, the RAEDAC comprising:

a parity generation circuit which receives, in any order, each bit of said string, and generates a plurality of parity bits, each related to a unique combination of said bits comprising said string;

a parity check circuit connected to said parity generation circuit to detect an error in a bit of said string using said parity bit; and

an error correction circuit coupled to the parity check circuit to correct said detected bit error.

32. (previously presented) The RAEDAC of claim 31 wherein the parity check circuit detects multi-bit errors in said string using said parity bits.

33. (previously presented) A random access error detection and correction (RAEDAC) unit for detecting and correcting errors in an ordered bit string of predetermined length, the RAEDAC comprising:

an error correction code generation circuit which receives, in any order, each bit of said string, and generates a plurality of check bits, each related to a unique combination of said bits comprising said string; and

an error detection circuit connected to said error correction code generation circuit to detect an error in a bit of said string using said check bits.

34. (previously presented) The RAEDAC of claim 33 further comprising:

an error correction circuit coupled to the error detection circuit to correct said detected bit error.

35. (previously presented) The RAEDAC of claim 33 wherein the error detection circuit detects multi-bit errors in said string using said check bits.

36. (new) The circuit of claim 24 wherein the bit stored in each cell is initialized to a selected value prior to operation of the circuit.

37. (new) The circuit of claim 27 wherein the bit stored in each cell is initialized to a selected value prior to operation of the circuit.